The 68HC11 Taxonomy

Revised 23:17 15/04/2017

Model	On-Chip Memory (bytes)				External Bus		Primary Timer				GPIO Pins [25,26]		Serial I/F	On-Chip 16-bit Arithmetic Co-Proc	A/D Convertor		D/A Convertor		H/W PWM [11,22]		on-chip bank-switched MMU	soft-configured chip-selects	Common Packages [19]	Motorola Temp. Grades	Comments
	RAM	ROM [1,3]	PROM [2,3]	EEPROM	Max. Avail. Freq. [18,23]	Multiplexed?	counter resolution	input capture channels	output compare channels	other primary-timer facilities	single-chip mode	expanded mode			channels	resolution	channels	resolution	channels	resolution					
HC11A0	256	-	-	-	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-	LCC-52, DIP-48, QFP-64	M, V, C	
L11A0 [15]	256	-	-	-	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-			
HC11A1	256	-	-	512	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-			
L11A1 [15]	256	-	-	512	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-			
HC11A7	256	8K	-	-	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-			
L11A7 [15]	256	8K	-	-	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-			
HC11A8	256	8K	-	512	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-			1st ever single-chip MCU containing EEPROM
L11A8 [15]	256	8K	-	512	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-			
HC811A2	256	-	-	2K [7]	2 MHz [8]	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-	LCC-52, DIP-48	0-70 Celcius	
HC811A8	256	-	-	512+8K	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-	LCC-52, DIP-48		
HC11B0 [4]	256	-	-	-		multiplexed					38/34 [12]	22/18 [12]	SCI, SPI	-			-	-	-	-	-	-		unspec	Requires 19V Vpp to program EEPROM
HC11B1 [4]	256	-	-	512		multiplexed					38/34 [12]	22/18 [12]	SCI, SPI	-			-	-	-	-	-	-			
HC11B3 [4]	256	8K	-	-		multiplexed					38/34 [12]	22/18 [12]	SCI, SPI	-			-	-	-	-	-	-			
HC11B8 [4]	256	8K	-	512		multiplexed					38/34 [12]	22/18 [12]	SCI, SPI	-			-	-	-	-	-	-			
HC11C0 [17]	256	-	-	-			16-bit	4/3	4/5	pulse acc, RTI, COP	50	33	SCI, SPI	-	4	8-bit	-	-	2	8-bit	Y (256Kb)	6	PLCC-68, PQFP-64	C	glueless memory interface (separate RE and WE signals, soft-configured chip-selects)
HC11D0	192	-	-	-	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	32/30 [9]	16/14 [9]	SCI, SPI	-	-	-	-	-	-	-	-	-	LCC-44, DIP-40, QFP-44	M,V,C	
HC11D3	192	4K	-	-	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	32/30 [9]	16/14 [9]	SCI, SPI	-	-	-	-	-	-	-	-	-			
L11D3	192	4K	-	-	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	32/30 [9]	16/14 [9]	SCI, SPI	-	-	-	-	-	-	-	-	-			
HC711D3	192	-	4K	-	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	32/30 [9]	16/14 [9]	SCI, SPI	-	-	-	-	-	-	-	-	-			
HC11ED0	512	-	-	-	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	n/a [20]	14/12 [9]	SCI, SPI	-	-	-	-	-	-	-	-	-	PLCC-44, DIP-40, QFP-44	M, V, C	
HC811E2 [13]	256	-	-	2K [7]	2 MHz	multiplexed	16-bit	3	5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	4 or 8 [12]	8-bit	-	-	-	-	-	-	LCC-52, DIP-48	0-70	
HC11E0	512	-	-	-	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-	LCC-52, QFP-64, DIP-48, SDIP-64, SDIP-56	M, V, C	
L11E0 [15]	512	-	-	-	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
HC11E1	512	-	-	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
L11E1 [15]	512	-	-	512	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
HC11E8	512	12K	-	-	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
L11E8 [15]	512	12K	-	-	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
HC11E9	512	12K	-	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
L11E9 [15]	512	12K	-	512	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
HC711E9	512	-	12K	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-			
S711E9	512	-	12K	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI, SPI	-	8	8-bit	-	-	-	-	-	-	LCC-52, QFP-64		forcibly disables on-chip OTPROM/ EPROM in expanded operation modes ("enhanced single-chip security").
HC11E18	768	-	-	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI+, SPI	-	8	8-bit	-	-	-	-	-	-	LCC-52, QFP-64	C	
HC11E20	768	20K	-	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI+, SPI	-	8	8-bit	-	-	-	-	-	-	LCC-52, QFP-64	M, V, C	
HC711E20	768	-	20K	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI+, SPI	-	8	8-bit	-	-	-	-	-	-			
HC11E32	768	32K	-	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI+, SPI	-	8	8-bit	-	-	-	-	-	-			
HC11EA9	512	12K	-	512	2.1 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI+	-	8	8-bit	-	-	-	-	-	-	LCC-52, PDIP-56	C	power-saving software-programmable voltage-controlled PLL clock circuit
HC711EA9	512	-	12K	512	2.1 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	38/34 [12]	22/18 [12]	SCI+	-	8	8-bit	-	-	-	-	-	-	LCC-52		
HC11F1	1024	-	-	512 [7]	5 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	54	38	SCI+, SPI	-	8	8-bit	-	-	-	-	-	4	LCC-68, TQFP-80	M, V, C	4XOUT clock output
L11F1 [15]	1024	-	-	512 [7]	3 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	54	38	SCI+, SPI	-	8	8-bit	-	-	-	-	-	4		M, V, C	4XOUT clock output
HC11FC0	1024	-	-	-	6 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	54	38	SCI, SPI	-	-	-	-	-	-	-	-	4	QFP-64, TQFP-80	0-70	DS pin, WAIT pin
L11FC0 [15]	1024	-	-	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	54	38	SCI, SPI	-	-	-	-	-	-	-	-	4		0-70	DS pin, WAIT pin
HC11FL0 [16]	1024	-	-	-		non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP?	70	54	SCI, SPI. Others?	-			-	-	-	-	-		100-pin		has ports I & J in addition to the normal 'F1 ports
HC11G0	512	-	-	-	2 MHz	non-multiplexed	16-bit	6/3	4/7	pulse acc, RTI, COP	66	42	SCI, SPI	-	8	10-bit	-	-	4	8-bit	-		PLCC-84		additional 16-bit timer (may be externally clocked); additional 3-channel event-
HC11G5	512	16K	-	-	2 MHz	non-multiplexed	16-bit	6/3	4/7	pulse acc, RTI, COP	66	42	SCI, SPI	-	8	10-bit	-	-	4	8-bit	-				

Assembled by Mike Spooner

The 68HC11 Taxonomy

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Model	On-Chip Memory (bytes)				External Bus		Primary Timer				GPIO Pins [25,26]		Serial I/F	On-Chip 16-bit Arithmetic Co-Proc	A/D Convertor		D/A Convertor		H/W PWM [11,22]		on-chip bank-switched MMU	soft-configured chip-selects	Common Packages [19]	Motorola Temp. Grades	Comments
	RAM	ROM [1,3]	PROM [2,3]	EEPROM	Max. Avail. Freq. [18,23]	Multiplexed?	counter resolution	input capture channels	output compare channels	other primary-timer facilities	single-chip mode	expanded mode			channels	resolution	channels	resolution	channels	resolution					
HC711G5	512	-	16K	-	2 MHz	non-multiplexed	16-bit	6/3	4/7	pulse acc, RTI, COP	66	42	SCI, SPI	-	8	10-bit	-	-	4	8-bit	-		PLCC-84		counter; MRDY/HALT bus-hold/clock-stretch control pin
HC11G7	512	24K	-	-	2 MHz	non-multiplexed	16-bit	6/3	4/7	pulse acc, RTI, COP	66	42	SCI, SPI	-	8	10-bit	-	-	4	8-bit	-				
HC11J6	512	16K	-	-	2 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	54		SCI, SPI	-	8	8-bit	-	-	-	-	-	1	SDIP-64, PLCC-68		
HC711J6	512	-	16K	-	2 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	54		SCI, SPI	-	8	8-bit	-	-	-	-	-	1			
HC11K0 [6]	768	-	-	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4	LCC-84, QFP-80	M,V,C	XOUT with configurable divisor [29]
L11K0 [6]	768	-	-	-	3 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
HC11K1 [6]	768	-	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
L11K1 [6]	768	-	-	640	3 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
HC11K3 [6]	768	24K	-	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
L11K3 [6]	768	24K	-	-	3 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
HC11K4 [6]	768	24K	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
L11K4 [6]	768	24K	-	640	3 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
HC711K4 [6]	768	-	24K	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	y (1Mb)	4			
HC11KA0 [5,10]	768	-	-	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI+	-	8	8-bit	-	-	4	8-bit	-	-	LCC-68, QFP-80	M,V,C	directly derived from K4; 4XOUT clock output
HC11KA1 [5,10]	768	-	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI+	-	8	8-bit	-	-	4	8-bit	-	-			
HC11KA3 [5,10]	768	24K	-	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI+	-	8	8-bit	-	-	4	8-bit	-	-	LCC-68		
HC11KA4 [5,10]	768	24K	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI+	-	8	8-bit	-	-	4	8-bit	-	-	LCC-68, QFP-80		
HC711KA4 [5,10]	768	-	24K	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI+	-	8	8-bit	-	-	4	8-bit	-	-			
HC11KA2 [5,10]	1024	32K	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	-	-	LCC-68, QFP-80	M,V,C	directly derived from K4; 4XOUT clock output
HC711KA2 [5,10]	1024	-	32K	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	-	-	LCC-68		
HC11KS2	1024	-	32K	640	5 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	-	-	LCC-68, TQFP-80		directly derived from K4; no MMU or chip-selects; additional power-saving mode; Tekmos only?
HC11KS8	1536	-	48K	640	5 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	51	26	SCI+, SPI	-	8	8-bit	-	-	4	8-bit	-	-			
HC11KW1	768	-	-	640		non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	80	56	SCI+, SPI+	-	10	10-bit	-	-	4	8-bit	y (1Mb)	4	TQFP-100	C	2 additional 16-bit timers (which can also be externally clocked), each with 3 output-compares and 1 switchable input-capture/output-compare; 4XOUT
HC11L0	512	-	-	-	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-	LCC-68, QFP-64	M,V,C	EEPROM/CONFIG block-protect; separate 5V power supply (AVcc) for ADC
L11L0	512	-	-	-	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		M,V,C	
HC11L1	512	-	-	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		M,V,C	
L11L1	512	-	-	512	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		M,V,C	
HC11L5	512	16K	-	-	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		M,V,C	
L11L5	512	16K	-	-	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		M,V,C	
HC11L6	512	16K	-	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		M,V,C	
L11L6	512	16K	-	512	2 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		M,V,C	
HC711L6	512	-	16K	512	3 MHz	multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	46	30	SCI, SPI	-	8	8-bit	-	-	-	-	-	-		V,C	
HC11M2	1280	32K	-	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62		2 SCI, SPI	y	8	8-bit	-	-	4	8-bit	-	-	LCC-84, QFP-80		key wake-ups; 4-channel internal DMA
HC711M2	1280	-	32K	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62		2 SCI, SPI	y	8	8-bit	-	-	4	8-bit	-	-			
HC11N4	768	24K	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62		SCI, SPI	y	12	8-bit	2	8-bit	6	8-bit	-	-	LCC-84, QFP-80		
HC711N4	768	-	24K	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62		SCI, SPI	y	12	8-bit	2	8-bit	6	8-bit	-	-			
HC11P0 [6]	1024	-	-	-	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	3 SCI, SPI	-	8	8-bit	-	-	4	8-bit			LCC-84	C	one SCI has MI-bus interface; power-saving programmable PLL-clock circuit
HC11P1 [6]	1024	-	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	3 SCI, SPI	-	8	8-bit	-	-	4	8-bit				C	
HC11P2 [6]	1024	32K	-	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	3 SCI, SPI	-	8	8-bit	-	-	4	8-bit				C	
HC711P2 [6]	1024	-	32K	640	4 MHz	non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	3 SCI, SPI	-	8	8-bit	-	-	4	8-bit				C	
HC11PA8	2048	48K	-	512			16-bit	4/3	4/5	pulse acc, RTI, COP	47	23	SCI, SPI	-	8	6/8-bit	-	-	-	-					
HC711PA8	2048	-	48K	512			16-bit	4/3	4/5	pulse acc, RTI, COP	47	23	SCI, SPI	-	8	6/8-bit	-	-	-	-					
HC11PB8	2048	48K	-	512			16-bit	4/3	4/5	pulse acc, RTI, COP	47	23	SCI, SPI	-	8	6/8-bit	-	-	-	-					
HC711PB8	2048	-	48K	512			16-bit	4/3	4/5	pulse acc, RTI, COP	47	23	SCI, SPI	-	8	6/8-bit	-	-	-	-					
HC11PH8	2048	48K	-	768		non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	2 SCI, 2 SPI	-	8	8-bit	-	-	4	8-bit			LCC-84, TQFP-112	C	1 SCI has MI-bus interface; PLL-clock circuit; key wake-ups; three 8-bit modulus timers; 4XOUT [24]
HC711PH8	2048	-	48K	768		non-multiplexed	16-bit	4/3	4/5	pulse acc, RTI, COP	62	37	2 SCI, 2 SPI	-	8	8-bit	-	-	4	8-bit				C	
HC11PM1 [27]																							QFP-128		
HC11S6	512	16K	-	640			16-bit	4/3	4/5	pulse acc, RTI, COP	70	46	SCI+, 2 SPI	-	8	8-bit	2	8-bit	4	?-bit			QFP-100, TQFP-100		32x4-seg LCD driver, Up/Down pulse counter
HC711S6	512	-	16K	640			16-bit	4/3	4/5	pulse acc, RTI, COP	70	46	SCI+, 2 SPI	-	8	8-bit	2	8-bit	4	?-bit					

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The 68HC11 Taxonomy

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Model	On-Chip Memory (bytes)				External Bus		Primary Timer				GPIO Pins [25,26]		Serial I/F	On-Chip 16-bit Arithmetic Co-Proc	A/D Convertor		D/A Convertor		H/W PWM [11,22]		on-chip bank-switched MMU	soft-configured chip-selects	Common Packages [19]	Motorola Temp. Grades	Comments
	RAM	ROM [1,3]	PROM [2,3]	EEPROM	Max. Avail. Freq. [18,23]	Multiplexed?	counter resolution	input capture channels	output compare channels	other primary-timer facilities	single-chip mode	expanded mode			channels	resolution	channels	resolution	channels	resolution					
HC11SA2 [27,28]																							QFP-128		

Notes:

* The list is ***not*** arranged in chronological order (which was somewhat chaotic in the early years); rather it is grouped by closely-related variants in approximate alphabetic group order.
* Highlighted italic values indicate values documented in one place, but not verified by (or contradicted by) a second reference - Mike S is in the process of rechecking the literature.
* Completely-blank items represent data for which a specific value has not yet been discovered.
* This document is *not* intended to describe *all* the differences between the various 6811 MCU models, only the primary feature differences. See the datasheets if you need full details.

\# Original 68HC11 design was heavily influenced by General Motors requirements (as was the predecessor NMOS 6801); especially the comprehensive timer and pin-capture/-compare facilities, programmable bus handshaking, on-chip EEPROM, SCI, and bootstrap mode.
\# Full-custom-VLSI 68HC11 MCUs have been manufactured by Motorola/Freescale/NXP and Toshiba (the latter using the Motorola mask-sets under licence).
Full-Custom-VLSI 68HC11A/D/E/L MCUs are still (2017) being manufactured (to order) by Rochester Electronics, using the Motorola/Freescale mask-set-designs under a transfer-of-intellectual-property arrangement.
Full-Custom-VLSI 68HC11A/D/E/F/K/KS MCUs are still (2017) being manufactured by Tekmos (using Tekmos mask-sets); but see note [3] re EPROM programming.
Various 68HC11 "soft" cores (eg: for implementing the MCU on an FPGA) have been available from several sources, including Digital Core Design and Green Mountain.
\# Contrary to many online comments, Motorola "XC" parts (eg: **XC**68HC11B0) are ***not*** "custom-mask/demo/broken/etc" versions;
For HCMOS components (eg: as opposed to the NMOS 6801 or HMOS 6805), the "XC" designation means that the part has not been completely formally qualified against published specifications for max/min temperature, max frequency, altitude, humidity, RFI.
ie: it is the purchasers responsibility to qualify (and if required by regulatory environment, document) each individual part for its' intended temperature/altitude/humidity environment and RFI parameters.
\# Some Motorola/Toshiba catalogues list the "Computer Operating Properly" (watchdog) facility using the term WDOG instead of COP (which is the term the datasheets use).

[1] excluding the additional 192- or 256-byte (mask-) BootROM that is only visible in special bootstrap mode.
[2] Software-programmable ROM. For parts in opaque packages, this is one-time-programmable ROM (OTPROM). For parts in windowed ceramic packages, this is U/V-erasable ROM (EPROM).
[3] Excepting 6811 MCUs manufactured by Tekmos, this is implemented as an EPROM array;
Tekmos 6811 MCUs contain an on-chip flash-based array instead of EEPROM, this requires different programming alorithm and voltage, but otherwise operates identically - see Tekmos app-notes for details.
In both cases, MCUs sold as "Mask-ROM" parts have this array factory-preprogrammed with customer-provided code/data or the BUFFALO monitor, and MCUs sold as "OTPROM" or "EPROM" parts ship with the array erased.
[4] Only available as partially-qualified "XC" parts (e.g. XC68HC11B), not formally qualified for critical-system use or at "M" military-spec temperature-range.
[5] Requires 19V Vpp to program the on-chip EEPROM, ie: does not use on-chip charge-pumps, unlike all other EEPROM-equipped 68HC11 MCUs which do not require Vpp for EEPROM.
[6] ROMAD configuration bit: soft-configurable on-chip-(EP)ROM base address - at either of two fixed base addresses.
[7] A2, E2 and F1 can soft-configure the base address of on-chip EEPROM to top half of any 4Kb block; the other 6811 models have static base addresses for EEPROM.
[8] Early mask-sets of 68HC11A2 could not execute out of EEPROM above 1MHz.
[9] On the DIP-40 package, PA4 and PA6 are not bonded to package pins.
[10] The KA-series were originally K-series dies squashed into an LCC-68 package for Delco Electronics. The MMU-related signals are not bonded to package pins.
[11] **All** 68hc11 MCUs provide "hardware-assisted" PWM facilities, but some additionally provide "fully-hardware-controlled" (setup-fire-and-forget) PWM facilities, which is what "H/W PWM" refers to here.
[12] On the DIP-48 package, PE4-PE7 (also used for ADC channels 4-7) are not bonded to package pins.
[13] The E**2** core was an intermediate design between (earlier) A-series and the other E-series MCUs - on-chip setup/devices not completely identical to E0/E1/E8/E9/E18/E20.
[14] DIP, LCC and QFP packages were each available in two variants for some 6811 MCUs: plastic (PDIP, PLCC, P-QFP) or ceramic (CDIP, CLCC, C-QFP).
[15] Extended-voltage part (full-speed operation over entire Vdd operating range 3.0V - 5.5V, as opposed to nominal Vcc of 5.0V required by other parts for full-speed operation).
[16] Not available to OEMs or retail: used only in some Motorola CDM radios; based on 68HC11F1 core but with extra ports and some noise reduction features; unusual BootROM address (0080).
[17] 68HC11**C0** was a special design for AT&T: glueless memory interface and on-chip MMU (upto 256Kb)
[18] Specific part number variants of each model were rated for specific max bus frequency, eg: there were 68HC11E1 parts rated for 2MHz, and other 68HC11E1 parts rated for 3MHz.
[19] A few 68HC11 models were also available in other packages, eg: Plastic SDIP.
[20] Does not have "single-chip" mode; or rather, only bootstrap-, test-, and expanded-mode are documented for it in the datasheet and technical reference.
[22] On the K-series, KW1, P1 and P2 (and possibly also on the KA-series), the 4-channel 8-bit PWM hardware can be soft-configured in 2-channel 16-bit mode.
[21] Numbers given here only apply to full-custom-VLSI 6811 MCUs;
Soft-core 6811 max bus frequency is dependant on the exact FPGA used and the exact soft-core structure: some FPGA-based 68HC11E MCUs have been qualified for 135MHz bus frequency.
[23] On the QFP-64 package, four signal-lines are not bonded to the package - probably PE4-PE7 (also used for ADC channels 4-7).
[24] On LCC-84 package, 4XOUT is not bonded to any package pin.
[25] On all 6811 MCUs, some general-purpose pins are output-only (Port B in particular), but they are still counted as "GPIO" in this document.
[26] Be very careful regarding GPIO pin-counts when reading Motorola catalogues and product-selection guides:
Motorola states the *expanded-mode* GPIO pin-counts for all MCUs lacking enabled on-chip ROM/PROM/EPROM, on the assumption that you would want to use an external ROM chip,
but states the *single-chip-mode* GPIO pin-counts for all MCUs with enabled on-chip ROM/PROM/EPROM, on the assumption that you would *not* want to use any external memory chips;
in the real world, neither of those assumptions necessarily hold (it's application-specific, after all); thus here GPIO pin-counts for *both* modes are *explicitly* stated.
[27] Mentioned in the 1996 Motorola internal "MICROCONTROLLER TECHNOLOGIES GROUP RELIABILITY AND QUALITY MONITOR REPORT" and also the 1997 Edition.
[28] Mentioned in the Freescale "PRODUCT DISCONTINUANCE NOTICE" dated 24-NOV-2004.
[29] On QFP-80 package, XOUT is not bonded to a package pin.

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